What Is Claimed Is:

Sub A1

1. A semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising:

a substrate of a first conductivity type forming a base for said semiconductor structure;

a first region of a second conductivity type within said substrate for forming a drain of a first MOS transistor;

a second region of the second conductivity type within said substrate for forming a source of the first MOS transistor;

a third region of the second conductivity type within said substrate coupled to a gate of a second MOS transistor, wherein

a fourth region of the first conductivity type is disposed adjacent to the third region of the second conductivity type for surrounding said first MOS transistor with an additional pick-up diffusion to reduce a turn-on speed or a longer channel length to increase a drain-base breakdown voltage of said first MOS transistor.

2. The semiconductor structure of claim 1, wherein said fourth region of the first conductivity type is disposed adjacent to the third region of the second conductivity type for surrounding said first MOS transistor with an additional pick-up diffusion to reduce a turn-on speed and a longer channel length to increase a drain-base breakdown voltage of said first MOS transistor.

3. The semiconductor structure of claim 1, further comprising:

a pre-buffer circuit coupled to said gate of the first MOS transistor; and

an output pad coupled to said first region of the first MOS transistor.

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4. The semiconductor structure of claim 1, further comprising:

a first channel region of the second conductivity type having a first channel length and disposed between said first and second regions of said first MOS transistor;

a second channel region of the second conductivity type having a second channel length and disposed between said first and third regions,

wherein said first channel length is greater than said second channel length to further increase the device breakdown voltage for reducing the turn-on speed of said first MOS transistor.

5. A semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising:

a substrate of a first conductivity type forming a base for said semiconductor structure;

a pair of first regions of a second conductivity type within said substrate for defining a first channel region of the second conductivity type for a first MOS transistor; and

a pair of second regions of the second conductivity type within said substrate for defining a second channel region of the second conductivity type for a second MOS transistor,

wherein the channel length of said first channel region is greater than the channel length of said second channel region to reduce a turn-on speed of said first MOS transistor

6. The semiconductor structure of claim 5, further comprising:

a pre-buffer circuit coupled to said first channel region; and

an output pad coupled to one of said pair of first regions of said second conductivity type and one of said pair of second regions of said second conductivity type.

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7. The semiconductor structure of claim 5, further comprising a third region of the first conductivity type adjacent to one of said second regions of said second conductivity type for surrounding said MOS transistor with an additional pick-up diffusion to further restrain the turn-on of said first MOS transistor

8. A semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising:

a p-type substrate of forming a base for said semiconductor structure;

a first N+ region within said substrate for forming a drain of a first MOS transistor;

a second N+ region within said substrate for forming a source of the first MOS transistor;

a third N+ region within said substrate coupled to a gate of a second MOS transistor, wherein

a P+ region is disposed adjacent to the third N+ region for surrounding said first MOS transistor with an additional pick-up diffusion to reduce a turn-on speed or a longer channel length to increase a drain-base breakdown voltage of said first MOS transistor.

9. The semiconductor structure of claim 8, wherein said P+ region is disposed adjacent to the third N+ region for surrounding said first MOS transistor with an additional pick-up diffusion to reduce a turn-on speed and a longer channel length to increase a drain-base breakdown voltage of said first MOS transistor.

10. The semiconductor structure of claim 8, further comprising:

a pre-buffer circuit coupled to said gate of the first MOS transistor; and

an output pad coupled to said first region of the first MOS transistor.

11. The semiconductor structure of claim 8, further comprising:

a first n-channel region having a first channel length and disposed between said first and second regions of said first MOS transistor;

a second n-channel region having a second channel length and disposed between said first and second regions,

wherein said first channel length is greater than said second channel length to further reduce a turn-on speed or a higher breakdown voltage of said first MOS transistor.

12. A semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising:

a p-type substrate forming a base for said semiconductor structure;

a pair of first N+ regions within said substrate for defining a first n-channel region for a first MOS transistor; and

a pair of second N+ regions within said substrate for defining a second n-channel region for a second MOS transistor, wherein

the channel length of said first channel is greater than the channel length of said second channel.

13. The semiconductor structure of claim 12, further comprising:

a pre-buffer circuit coupled to said first channel region; and

an output pad coupled to one of said pair of first N+ regions and one of said pair of second N+ regions.

14. The semiconductor structure of claim 12, further comprising a third region of the first conductivity type adjacent to one of said second N+ regions for surrounding said MOS transistor with an additional pick-up diffusion to further restrain the turn-on speed of said first MOS transistor.

15. A semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit, said semiconductor structure connected between an input pad and an internal circuit of said integrated circuit and comprising:

a substrate of a first conductivity type forming a base for said semiconductor structure;

a first channel of a second conductivity type formed between first regions of said second conductivity type within said substrate for a first MOS transistor; and

a second channel of the second conductivity type formed between second regions of said second conductivity type within said substrate for a second MOS transistor, wherein

an additional pick-up diffusion region is disposed adjacent to said first regions of said second conductivity type to reduce a turn-on speed or increase a drain breakdown voltage of said first MOS transistor.

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16. The semiconductor structure of claim 15, wherein the channel length of said first channel is greater than the channel length of said second channel.

17. A semiconductor structure for electrostatic discharge (ESD) protection of a high-voltage tolerant I/O cells with stacked NMOS or PMOS integrated circuit, said semiconductor structure connected between a pre-driver circuit and an input/output pad of said integrated circuit and comprising:

a substrate of a first conductivity type forming a base for said semiconductor structure;

a first channel of a second conductivity type formed between first regions of said second conductivity type within said substrate for a first MOS transistor which is stacked on a third MOSFET of a second conductivity type; and

a second channel of the second conductivity type formed between second regions of said second conductivity type within said substrate for a second MOS transistor which is stacked on a fourth MOSFET of a second conductivity type, wherein

an additional pick-up diffusion region is disposed adjacent to said first regions of said second conductivity type to reduce a turn-on speed and/or a longer channel length to increase a drain-base breakdown voltage of said first MOS transistor.

18. The semiconductor structure of claim 17, wherein the channel length of said first channel is greater than the channel length of said second channel.

19. A semiconductor structure for electrostatic discharge (ESD) protection, comprising:

at least one ESD protection device; and

at least one guarded device which is turned-on by a turn-on restrain means, wherein the ESD protection device can be turned-on before the guarded device is turned-on.